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**Bridges, K.G. / Chopra, R. / Lin, L. / Svenson, K. / Tam, A. / Jin, G. / Cowling, R. / (...) / DiBlasio-Smith, E.**, *Peptides*, Jul 2006

@b-Secretase 1 (BACE1) is an aspartic protease believed to play a critical role in Alzheimer's disease. Inhibitors of this enzyme have been designed by incorporating the non-cleavable hydroxyethylene and statine isosteres into peptides...

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**Pomogailo, S.I. / Shilov, G.V. / Ershova, V.A. / Virovets, A.V. / Pogrebnyak, V.M. / Podberezhskaya, N.V. / Golovin, A.V. / (...) / Pomogailo, A.D.**, *Journal of Organometallic Chemistry*, Oct 2005

...capable to producing an activation of N-allylic substrates resulted in their double-bond [1,2]-migration and simultaneous **intra-substrate** hydrogen transfer[2]. While the catalytic properties of the mentioned complexes, in particular in alkene's oxidation...

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3. [Molecular dynamics simulation on burst and arrest of stacking faults in nanocrystalline Cu under nanoindentation](#)

**Xin-Ling Ma / Wei Yang**, *Nanotechnology*, Nov 2003

...unit vector with direction from tip sphere centre K to substrate atom i. Functions VI(r<sub>j</sub>) and VE(r<sub>iK</sub>) are the **intra-substrate** and interfacial atomic potentials, respectively. Numerical integration of equation (1) was accomplished via a leap-frog...

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4. [TILT SENSOR APPARATUS AND METHOD THEREFOR](#)

**MORRISON, Christopher, S. / NUVO HOLDINGS, L.L.C., PATENT COOPERATION TREATY APPLICATION**, Sep 2005

...middle substrate 38. An opening wall 52 surrounds opening 46 and extends between bottom and top surfaces 48 and 50. An **intra-substrate** conductor 54 resides on opening

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...the wafer scribe area, adjacent to the **active** portion of the chips.

&lsqb;0006&rsqb;...exclude the scribe area adjacent to the chip **active** area.

&lsqb;0007&rsqb; Still further...little information on components in the **active** area chip areas of the wafer. For example...

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(May 2004) Sagar Suresh Sabade, B.E., Pune University, India; M.Tech., Indian Institute of Science, Bangalore, India Chair of Advisory Committee: Dr.

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...engineers are dazzled by an increasing **intra-die** variability for which no obvious...example, to tackle the problem of **intra-die** variability, system designers will...flow compatible with the standard **wire bonding** technology. In addition to the...  
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2. [1\\_title \[PDF-137K\]](#)

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...Exposure & Strip Ion Implant Ion Implant Metal Deposition Metal Deposition Layout Design Layout Design TEST TEST **Wire Bonding** **Wire Bonding** Packaging Packaging Lecture on Advanced CAE Jeong-Taek Kong 1 - 5 Introduction Traditional TCAD Wafer...  
[<http://asic.postech.ac.kr/3.Class/1.Classes/samsung695...>]  
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3. [SPIE Proceedings Vol. 2874 \[63K\]](#)

Oct 1996

...manufacturing (Paper #: 2874-01) \* Inter- and **intra-die** polysilicon critical dimension variation...practice. !23 Paper #: 2874-02 Inter- and **intra-die** polysilicon critical dimension variation...the relative range and distribution of **intra-die**, or die-level, polysilicon critical dimension...  
[<http://www.spie.org/web/abstracts/2800/2874.html>]  
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4. [A unified switching theory with applications to VLSI design - John P. Hayes, Proc. IEEE 70 \(10\), 1140 \(1982\)](#)

*Microelectronics Reliability*, Jan 1983

...discussed in Part II. Thermosonic gold **wire bonding** to copper conductors. VERNON A...hybrid microcircuitry requires that **wire bonding** to their surfaces be demonstrated...of critical layers. Excellent **intra-die** overlay match is demonstrated...

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5. [METHOD AND APPARATUS FOR NON-CONDUCTIVELY INTERCONNECTING INTEGRATED CIRCUITS](#)

**KNIGHT, Thomas, F. / SALZMAN, David, B. / KNIGHT, Thomas, F., PATENT**

*COOPERATION TREATY APPLICATION*, Jan 1995

...flip-chip, tape automatic bonding (TAB), or **wire-bonding**. In the MCM-C technologies,

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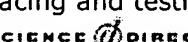
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**ter Brake, H.J.M. / Buchholz, F.Im. / Burnell, G. / Claeson, T. / Crete, D. / Febvre, P. / Gerritsma, G.J. / (...) / Ivanov, Z.**, *Physica C: Superconductivity and its applications*, Jun 2006  
The roadmap gives an overview on status and future developments in Superconducting Digital Electronics (SDE). Key areas in SDE under focus are applications, circuit simulation and design, circuit fabrication, interfacing and testing,....  
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...measurement equipment, and it is typically shorter than local **wiring** delay. Cascading 1 cells with minimum interconnects has the...application, we used the test chip to evaluate the effect of **intra-wafer** process variations. To this purpose we measured the variations...  
[<http://www.sti.uniurb.it/bogliolo/e-publ/isqed03.pdf>]  
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**Buchholz, F.-I. / Balashov, D. / Khabipov, M.I. / Hagedorn, D. / Dolata, R. / Popel, R. / Niemeyer, J.**, *Physica C*, Feb 2001

...layer enabling contacts of the Nb top **wiring** to the junction top electrode (central...characteristics (hysteresis: less than 7%), the **intra-wafer** parameter spread for j C is below...small contact holes and connecting a **wiring** layer within these holes without...)

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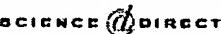
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...uniformity, but gives considerable **intrawafer** variation [2]. The SOG-based process exhibits much better **intrawafer** uniformity than CMP, but shows...ring oscillator speed with **wiring** loading across a wafer.  
The...useful in capturing the severe **intrawafer** dielectric thickness variation...  
[<http://inst.eecs.berkeley.edu/~ee290h/fa03/handouts/Yi...>]  
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2. [SINIS fabrication process for realizing integrated circuits in RSFQ impulse logic](#)  
**D Balashov / M I Khabipov / F-Im Buchholz / W Kessel / J Niemeyer**, *Superconductor Science and Technology*, Nov 1999  
...corresponding to LS = 0.94 pH (**wiring**-ground), 0.71 pH (**wiring**-base) and 0.58 pH (base-ground) with **intrawafer** margins of LS = ±0...different types of **wiring** connection (see section...less than 10%) the **intrawafer** parameter spread is...

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*Microelectronics Reliability*, Jul 1993...specifically, this paper presents the algorithms for the analysis of **intrawafer** variability. Measurements are made on many individual devices...array makers who offer custom products by changing only the **wiring** process. Thus creating custom standard cells involves only...**Published journal article available from** 



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